Intel® Ethernet Controller X710/XXV710/XL710

Dynamic Device Personalization L2TPv3 Over IP Protocols

Ethernet Products Group (EPG)

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Revision 1.4

Revision History

Revision	Date	Comments
1.4	July 2020	Added new device ids, added RSS support for PCTYPES 28 and 38.
1.3	December 2019	Updated Table 1-6.
1.2	July 2019	Updated Table 1-2 and 1-3.
1.1	June 24, 2019	Final version.
1.0	June 7, 2019	Initial release (Intel Confidential).

1.0   Introduction

This document describes the Dynamic Device Personalization (DDP) functionality supported by the Intel® Ethernet Controller X710/XXV710/XL710 starting with firmware version 6.01.

The DDP profile (0x80000004) contains the X710/XXV710/XL710 parser graph for L2TPv3 over IPv4 and IPv6 protocols.

Table 1-1. Terms and Definitions

Term	Definition
DDP	Dynamic device personalization.
L2TPv3	Layer 2 tunneling protocol, version 3.
IPv4	Internet Protocol, version 4.
IPv6	Internet Protocol, version 6.

Table 1-2. Version History

Version	Description
0.0.0.4	Initial release of L2TPv3 parser graph for the X710/XXV710/XL710 supporting both IPv4 and IPv6 transports.
1.0.0.0	Release of L2TPv3 parser graph for the X710/XXV710/XL710 supporting both IPV4 and IPV6 transports.

Table 1-3. Firmware/NVM Support Matrix

FW Version	NVM Map Version	Description
6.01	6.36	
6.02	6.48	Operating system and device independent.
7.0	8.77	

Table 1-4. L2TPv3 Packet Field Vector

Word Num	Protocol Layers			
	L2 Protocol Layers			
0:2	Destination MAC address (in outer or single L2 header)			
3:5	Source MAC address (in outer or single L2 header)			
6	Default S-tag (DPDK: word 37)			
7	0x00.			
8	Inner or single VLAN tag (in outer or single L2 header)			
	L3 Protocol Layers			
	L2TPv3 over IPv4		**L2TPv3 over IPv6**	
9	First eight words of the IPv4 header (up to including the source IP address)		First four words of the IPv6 header (up to including the hop limit)	
10				
11:12				
13:16			IPv6 source address	
17:20	0x00			
21:22	0x00		IPv6 destination address	
23:26	0x00			
27:28	Destination IP address			
	L4 Protocol Layers			
29:30	0x00			
31:32	0x00			
33:36	0x00			
	DPDK Outer VLAN for QinQ			
37	S-tag (DPDK)	S-tag (DPDK)	S-tag (DPDK)	S-tag (DPDK)
	L2TPv3 Pseudo-wire Layer and Flexible Payload			
38:43	0x00			
44:45	L2TPv3 Session ID			
46	0x00			
	Tunnel Layer and Flexible Payload			
47	0x00			
48	0x00			
50:57	Flexible payload			

Note: DPDK (up to release 17.11) forces the flexible payload to the first 16 bytes of the payload and overrides the outer destination IP address. Starting from DPDK 18.02, the flexible payload is extracted only if enabled by the flow director configuration.

Table 1-5. Packet Classifier Types and Its Input Set

PCTYPE	PCTYPE Description	Hash Input Set	FD Input Set
28	IPv4, L2TPv3	L2TPv3 Session ID	L2TPv3 Session ID
38	IPv6, L2TPv3	L2TPv3 Session ID	L2TPv3 Session ID

Note: L2TPv3 over UDP transport not supported.

Table 1-6. Packet Types

PTYPE	Description	PTYPE	Description
167	IPv4, L2TPv3, PAY4	168	IPv6, L2TPv3, PAY4

Note: L2TPv3 control message packets with Session ID 0 are not classified; Intel® Ethernet Flow Director or switch filter can be used for control message packets separation.

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